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THERMAL INVESTIGATION OF THREE-DIMENSIONAL GaN-on-SiC HIGH ELECTRON MOBILITY TRANSISTORS

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Final Report

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14. ABSTRACT
Wide-bandgap materials (e.g., GaN, SiC, and ZnO) have been widely used in many DoD applications, including integrated radio frequency (RF) amplifiers and power electronics. However, inherent inefficiencies in energy conversion and the continual push for underlying device performance have resulted in rapidly escalating heat generation rates in the near-junction region of these devices. One barrier for improving the thermal design of these devices is the multi-domain simulation problem of coupling electron transport and carrier statistics, phonon transport and populations, and ultimately full-wave electromagnetic solvers. A predictive simulation paradigm that follows energy transport at the fundamental carrier level to useful signal output and thermal dissipation is significantly beyond the state of the art for any single simulation capability.
In this project, electron and phonon Monte Carlo simulations (nanometer to micrometer scale for near-junction regions) and conventional Fourier-law-based heat transfer simulations (macroscopic devices) are combined to yield reliable thermal predictions for two-dimensional and three-dimensional GaN-on-SiC transistors. This multi-length-scale simulation strategy will introduce unprecedented insight into the heat generation and transport within a transistor and further relate the discovery to the thermal management of the whole device. This project provides important guidance for thermal management solutions, such as adding high-thermal-conductivity layers near the device junctions, engineering near-junction interfacial thermal resistances, and using micro-channel coolers. The success of this project can also significantly benefit many existing military and civil applications to improve the lifetime and reliability of three-dimensional devices.

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1. SUMMARY

This project aims to develop a hybrid simulation technique for electrothermal studies of high-power GaN devices, which includes both macroscale heat spreading across a macroscale chip and nanoscale electron and phonon transport. In this final report, the scheme of the developed simulation technique is described. In demonstration, the simulation technique has been applied to 2D GaN high electron mobility transistors and 3D field effect transistors based on an array of parallel GaN nanowires. In addition, 2D high electron mobility transistors with an AlN heat spreader on its top are simulated to check the temperature drop after adding this heat spreader. As another thermal management strategy, thermoelectric cooling using GaN alloys is studied, with a focus on how nanopores can be introduced to decrease the thermal conductivity of such alloys.

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2. INTRODUCTION

In recent years, tremendous efforts have been dedicated to GaN-based transistors for high-power and high-frequency applications. In a GaN high electron mobility transistor (HEMT),[1] two-dimensional electron gas (2DEG) is formed on the interface between GaN and its ternary alloy. With its high carrier mobility and carrier density, such 2DEG can transport a large current for power electronics. Beyond layered structure transistors, field effect transistors (FETs) using a GaN nanowire[2] or an AlGaN/GaN nanowire[3,4] have been widely studied because of improved output power, better gate controllability, and shorter channels for speedup and miniaturization. Compared to the fin-shaped FETs with nanowires placed on a planar substrate and gate on three sidewalls, vertical nanowires with a wrapped gate can provide even better gate controllability and shorter channels.[5,6] Despite the promising applications, GaN-based transistors still suffer from overheating within the device, which can reduce the electron mobility and thus the output power. Along this line, accurate electrothermal simulations are still lacking and can hinder future development of such transistors.

One challenge of electrothermal simulations for general nanoscale transistors lies in the complicated electron and phonon transport within the transistor region. Such transport processes include electron acceleration by the high electric field, optical phonon emission by hot electrons, decay of non-propagating optical phonons into acoustic phonons, and acoustic phonon transport across the whole macroscale chip. In many studies on GaN devices, the Fourier's law is used for the thermal simulations though the coupled electron transport studies have been improved from conventional drift-diffusion and hydrodynamic models[7,8] to advanced electron Monte Carlo (MC) simulations.[9,10] A review can be found for existing modeling work.[11] Despite more accurate predictions for electron transport, the Fourier's law becomes invalid when the structure size is comparable or even smaller than the phonon mean free paths (MFPs). The thermal conductivity k of a material region can be dramatically reduced from the bulk value due to boundary or interfacial scattering of phonons, which can impede phonon transport within the device and create challenges for thermal managements.[12] Recent studies have shown that phonons with MFPs greater than 1000±200 nm, 2500±800 nm, and 4200±850 nm contribute 50% of the room-temperature thermal conductivity k of bulk GaN, AlN, and 4H-SiC, respectively.[13] In this situation, Fourier's law analysis using bulk k values for different material regions yields underpredicted temperature rise within GaN-based nanotransistors. Accurate temperature predictions should be obtained by solving the phonon Boltzmann transport equation (BTE).[14] However, the distribution function f in the phonon BTE depends on many parameters, including phonon branch, phonon frequency, traveling direction, and locations. Considering the multidimensional nature of f, directly solving the BTE to obtain f can be extremely challenging. For three-dimensional structures, such calculations can be more complicated, particularly when phonon scattering by various interfaces are considered. As an alternative method to solving the phonon BTE, a new deviational phonon MC technique[15,16] enables accurate thermal simulations of general nano- to micro-electronics. By tracking the phonon movement and scattering within the device, the solution for the phonon BTE can be obtained statistically. This allows accurate electrothermal studies of high-power electronic devices such as GaN transistors.

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To study the heat spreading across the whole sub-mm chip, the phonon MC simulations are further coupled with Fourier's law analysis for regions away from the hot spot. This hybrid simulation technique can well address the energy transport over multiple length scales, ranging from the nanoscale transistor region to the macroscale substrate.

The milestones for this project are listed below. All five tasks have been accomplished on time.

Task 1 - Electron MC Simulation for Heat Generation within the Nanochannel
The performer shall develop the electron MC simulation technique to accurately predict the phonons emitted by hot electrons along a 1D nano-channel. The performer shall test the electron MC simulations by reproducing the electron drift velocity versus electric-field curve of bulk GaN at different lattice temperatures and comparing to those in the literature.

Task 2 - Phonon MC Simulation Coupled with Fourier Analysis
The performer shall incorporate phonon frequency dependency into phonon MC simulations of a 3D transistor and further couple the simulation with conventional Fourier analysis for the whole macro-scale device. The performer shall show the temperature distributions across the whole device, with specified phonon generation along the nano-channel and use the data to derive the device thermal resistance as the maximum temperature rise within the device for a given average dissipated power.

Task 3 – Electro-Thermal Simulations
The performer shall integrate the electron MC simulations and phonon-MC-Fourier solver for 3D transistors. The performer shall demonstrate converged temperature profile for operating 3D GaN-on-SiC HEMTs and improved computational efficiency with parallel computing.

Task 4 - Electromagnetic Thermal Simulations
The performer shall further incorporate electromagnetic heating effects into the electro-thermal simulations. The performer shall demonstrate electromagnetic-thermal simulations of a 3D GaN-on-SiC HEMT.

Task 5 - Simulation Confirmation
The performer shall use electro-thermal or electromagnetic-thermal simulations to explain the existing device performance data (e.g. output power) of 3D GaN-on-SiC HEMT and other 2D GaN-on-SiC HEMTs. The performer shall compare simulation results and existing experimental data.

This report is organized in the following way. In Section 3, the method of the coupled electrothermal simulation is explained. In Section 4, the simulation results are presented, which includes a 2D GaN/AlGaN HEMT under high electric field, a 2D HEMT with AlN heat spreader on top, and a 3D GaN FinFET array on SiC substrate. Thermal studies of nanoporous $In_{0.1}Ga_{0.9}N$ films are briefly discussed. Conclusions are given in Section 5.

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3. METHODS

Figure 1 shows the flow chart of the hybrid simulation technique that can fully incorporate energy-dependent phonon and electron transport.[11,17] The rough temperature distribution across the whole macroscale device is first obtained from ANSYS simulations using the Fourier's law and local volumetric heat generation rate Q''' extracted from electron MC simulations. On the boundary of the phonon MC domain, acoustic phonons are assumed to be in thermal equilibrium with the local temperature from ANSYS simulations. The temperature distribution within the phonon MC domain is then refined with phonon MC simulations that track the movement and scattering of individual phonon bundles. The obtained temperature T_A for acoustic phonons and temperature T_{LO} for longitudinal optical (LO) phonons are fed back into the coupled electron MC simulations to update the temperatures for the calculations of electron scattering rates. These simulations are carried out in an iterative way until convergence.

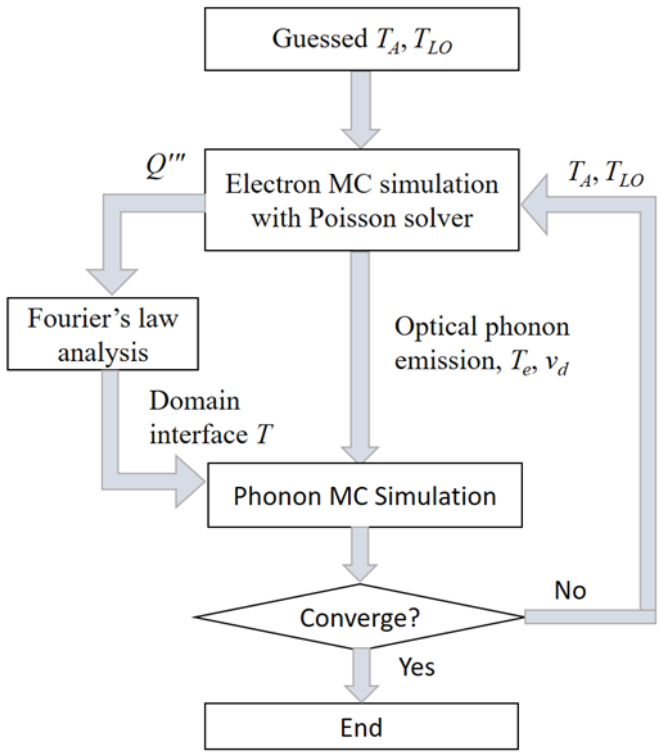

Figure 1: Flow Chart of the Hybrid Simulation Technique

3.1 Electron MC Simulation

Electron MC simulations are used to predict phonons emitted by hot electrons in GaN transistors. Under a high electric field, the topmost longitudinal optical phonons are emitted at 91.2 meV, whereas acoustic phonon scattering of electrons is assumed to be elastic. Such treatment is common in existing electrothermal studies on GaN devices.[7]

The computational domain is divided into many spatial bins called subcells. Charge neutrality is enforced at both ends of a GaN transistor (e.g., 2DEG channel or a nanowire), which is a typical treatment for metal or heavily doped semiconductor junctions. For 3D GaN FinFETs, diffusive

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electron scattering is assumed on the nanowire boundary. The local electron temperature T_e is computed by the thermal energy density of these carriers within each subcell.[10] Within each time step, the energy exchange between electron and LO phonons is recorded within each subcell. The volumetric heat generation rate is computed for each subcell and passed to Fourier's law analysis and phonon MC simulations.

3.1.1 Electronic Band Structure

The lowest three conduction band valleys of wurtzite GaN, known as the Γ_1, U, and Γ_3 valleys,[18,19] are considered in electron MC simulations. The electronic band structure is described by an analytical nonparabolic model, $E_i(1+\alpha_i E_i) = \hbar^2 k^2/2m_{0,i}$, where α is band nonparabolicity, E is the kinetic energy, $m_{0,i}$ is the effective mass at the valley minima, and i is index for the three valleys. Within a valley, the effective mass depends on E as $m_i = (1+2\alpha_i E_i)m_{0,i}$.[20]

Subbands in 2DEG

In GaN HEMTs, 2DEG forms at the interface between GaN and a thin layer of $Al_xGa_{1-x}N$. Perpendicular to the 2DEG plane, electrons are confined in an approximately triangular quantum well so that their energy associated with this direction is quantized.[21] Figure 2 shows the band diagram along this cross-plane direction and the lowest 10 quantized energy levels, as computed by solving the coupled Poisson equation and Schrödinger Equation. The calculations are conducted with the open-source AQUILA code written in MATLAB.[22] The considered junction is formed by depositing a 30-nm-thick $Al_{0.3}Ga_{0.7}N$ layer on a thick GaN layer. The n-type doping levels are 1×10^{15} cm^{-3} and 1×10^{17} cm^{-3} for GaN and AlGaN, respectively. The subband energies are calculated with a grounded gate. Referring to the energy of the lowest subband for a valley, the energies of the lowest five subbands of the valley are 0, 107, 150, 173, and 189 meV for the Γ_1 valley, 0, 94, 131, 153, and 168 meV for the U valley, and 0, 77, 111, 131, and 146 meV for the Γ_3 valley.

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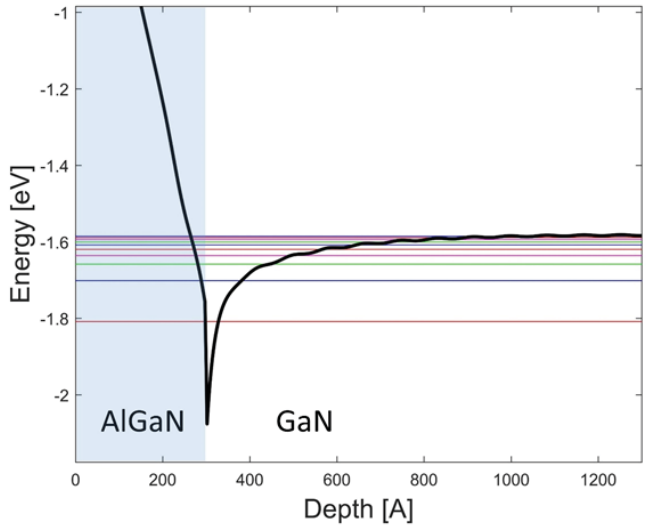

Figure 2: The Lowest 10 Quantized Energy Levels for 2DEG in the Γ_1 Valley of an $Al_{0.3}Ga_{0.7}N$/GaN Heterojunction

Shaded region on the left is the 30-nm-thick AlGaN layer and unshaded region on the right is 100-nm-thick GaN. The thick black line is the calculated conduction band edge.

When a high electric field (up to ~3×10^8 V/m) is considered, electrons are excited to higher energy levels and thus activate more subbands. In experiments, electron temperatures can be up to ~10000 K, which corresponding to ~0.9 eV as the thermal energy.[23,24] In this case, multiple subbands for each valley should be considered in electron MC simulations. To balance the accuracy and efficiency, the combination of five subbands for the Γ_1 valley, five subbands for the U valley, and two subbands for the Γ_3 valley has been adopted for all 2D GaN HEMT simulations. Further increasing the number of subbands does not affect the simulation results. The computed electric-field-dependent drift velocity at 300 K is shown in Figure 3. A peak drift velocity around 2.5×10^7 cm/s is reached at an electric field around 150 kV/cm. The general trend agrees well with previous electron MC simulations.[25,26]

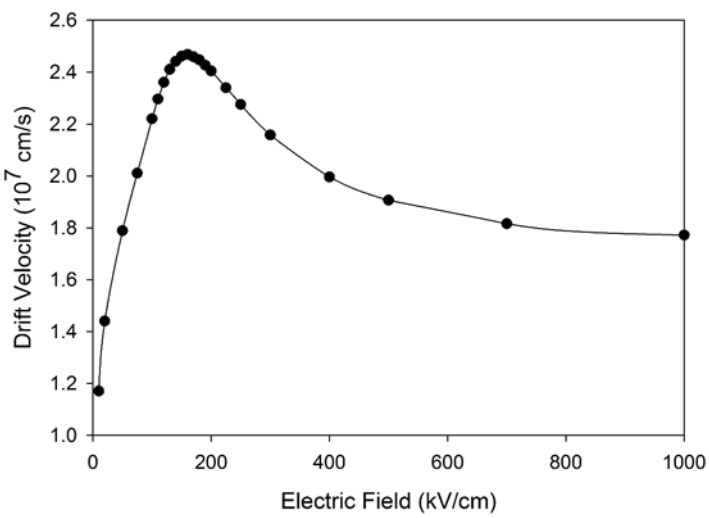

Figure 3: Electron Drift Velocity as a Function of Electric Field in a GaN HEMT at 300 K from Electron MC Simulations

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3.1.2 Electron Scatterings

The electron scattering mechanisms include polar optical phonon scattering, ionized impurity scattering, acoustic deformation potential scattering, and intervalley optical phonon scattering. The exact expressions for the scattering rates of these scattering mechanisms can be found elsewhere.[17,27,28] For GaN HEMTs, since the 2DEG is confined on the undoped GaN side of the heterojunction, ionized impurity scattering is not considered. The important parameters are listed in Table 1.

Table 1. Parameters used in Electron MC Simulations

Parameter	Symbol	Value
Electron effective mass (m_e)	$m_{0,i}$	0.21, 0.25, 0.40
Valley minimum energy (eV)	$E_{c,i}$	0, 1.95, 2.1
Nonparabolicity (eV^{-1})	α	0.19, 0.10, 0
Dielectric constant (ε_0)	$\varepsilon_s, \varepsilon_\infty$	8.9, 5.35
Mass density (g/cm^3)	ρ	6.095
Acoustic deformation potential (eV)	D_a	8.3
Intervalley deformation potential (eV/cm)	D_{ij}	1.0×10^9

3.1.3 Electric Field Calculation

The electric field **E** within electron MC simulation domain is initially computed by ATLAS using the drift-diffusion model for electron transport. Using this initial electric field, electron MC simulation is performed and the charge density ρ_e in the electron MC simulation domain is calculated after the steady state is reached. The electric field within the computational domain is updated at the end of each step by solving the Poisson equation $\nabla^2\Phi = -\rho_e/\varepsilon$. Different from electron MC simulations, the Poisson solver considers the whole device structure. The electric field can then be derived from the potential Φ as $\mathbf{E} = -\nabla\Phi$. The local charges include ionized impurities and mobile electrons. As the boundary condition, the gradient of Φ along the normal direction of all surfaces is zero without surface charges.[29] Interfacial charges are also neglected in the Poisson solver.

3.2 Phonon MC Simulation

Energy-dependent phonon transport is studied with phonon MC simulations that are coupled with electron MC simulations. In conventional phonon MC simulations, accurate temperatures can be statistically obtained with sufficient phonon bundles to count the phonon energy density within each subcell.[30,31] Such requirements create problems for the simulated structure with large contrast between the sizes of a single subcell and the micron computational domain. Billions of phonon bundles are required for the whole computational domain so that sufficient phonon bundles can still be found within each subcell to accurately predict the hot spot inside the transistor. This requirement cannot be satisfied with the computational capacity of typical computers, particularly when the phonon MC simulations are further coupled with other simulations in the hybrid technique. This issue has been resolved with a new deviational phonon

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MC technique developed by Péraud and Hadjiconstantinou.[15,16] Instead of tracking all phonons, this new technique only tracks phonons related to the deviation of the phonon distribution function f from the equilibrium f_0 (i.e., Bose-Einstein distribution) at a reference temperature. More deviation phonons bundles are thus distributed near the hot spot and very few bundles are required for the region close to the reference temperature. Less than 100 million phonon bundles are typically required for electronic devices with sizes up to ~10 μm.

3.2.1 Phonon Dispersion and Scattering Rates

As input parameters, an isotropic sine-shaped phonon dispersion (i.e., Born-von Karman dispersion) is used for all materials. The sine dispersion is better than the Debye model, as it captures the dispersion features both at low and high ends of the frequency range. All optical branches are assumed dispersionless so that they do not contribute to heat conduction due to zero phonon group velocities. For three identical acoustic branches, the phonon angular frequency ω and wave vector q are related by $\omega = \omega_{\max}\sin(\pi q/2q_0)$, in which $\omega_{\max}$ and q_0 are the maximum ω and q value, respectively. Here q_0 and the equivalent atomic distance a_D can be calculated using $q_0 = \frac{\pi}{a_D} = (6\pi^2 N)^{1/3}$, with N as the volumetric density of primitive cells. The maximum angular frequency can be calculated from the sound velocity v_s as $\omega_{\max} = \frac{2v_s}{a_D}$. The essential phonon scattering mechanisms in all related materials are impurity scattering and the Umklapp process of the phonon-phonon scattering. The combined phonon relaxation time $\tau(\omega)$ is given as $1/\tau(\omega) = A\omega^4 + B_1\omega^2 T\exp(-B_2/T)$, where the first term on the right side is for impurity scattering and the second term is for Umklapp scattering. Parameters used for all materials are obtained by fitting measured thermal conductivities and are listed in Table 2. The obtained temperature-dependent k_L and phonon MFP distribution agree well with experimental results.[13,17,32] For heavily doped GaN as in 3D GaN FinFETs, electron scattering of phonons should also be considered.[33]

Table 2. Parameters used in Phonon MC Simulations

Parameter	GaN	$Al_{0.3}Ga_{0.7}N$	SiC	AlN	Al_2O_3	Au
k_0 (10^9 m^{-1})	10.94	10.99	8.94	11.19	8.838	15.18
$\omega_{\max}$ (10^{13} rad/s)	3.50	3.99	7.12	5.18	4.0943	3.13
a_D (Å)	2.87	2.86	3.51	2.81	3.55	2.07
A (10^{-45} s^3)	5.26	817	1.00	10.5	72.91	3189
B_1 (10^{-19} s/K)	1.10	0.421	0.596	0.728	3.55	1495
B_2 (K)	200.0	239.1	235.0	287.5	122.9	59.8

3.2.2 Optical Phonon Temperature Determination

Within each time step, new acoustic phonons are generated by the decay of optical phonons emitted by hot electrons. A constant relaxation time of 2 ps is used for the decay of optical phonons.[34] In steady states, the total energy of acoustic phonons matches the energy of emitted optical phonons within each subcell. This energy balance for optical phonons can be further used to determine T_{LO}.[10,17] The energy and branch of emitted acoustic phonons are randomly set based

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on the local temperature of optical phonons. Similar phonon setting based on a given temperature can be found elsewhere.[30,35,36]

3.3 Coupling Phonon MC Simulation with Fourier's Law Analysis

At the interface between the phonon MC domain and its surrounding Fourier domain, phonons are assumed to be in thermal equilibrium with the local temperature.[15] The temperature profile on this domain interface is determined by Fourier's law analysis using heat generation from electron MC simulations. For the rest of the phonon MC domain boundary (i.e., the top surface of the device), diffusive reflection is enforced for incident phonons. The exact treatment of internal and interfacial phonon scattering can be found in the literature.[30,35,36] The thermal resistance of the GaN-sapphire interface is further computed based on the phonon transmissivity from the diffusive mismatch model.[37] This resistance is used in the Fourier's law analysis for better accuracy.

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4. RESULTS

4.1 2D GaN HEMT

A 2D GaN HEMT featuring a four-layered structure is illustrated in Figure 4. From the top to the bottom, the layers are a 30-nm-thick AlGaN layer, a 2.5-µm-thick GaN layer, a 60-nm-thick AlN nucleation layer, and the substrate SiC with 500 µm thickness. The source, gate, and drain are on top of the AlGaN layer, and are all 1 µm wide, and separated by 1 µm. The horizontal length of the whole device is chosen to be 500 µm. The electron MC simulation is only carried out for the 2DEG between the source and drain, with the channel length of 3 µm. Both the source and the gate are grounded, and a 15 V voltage is applied to the drain. The electric field is peaked right at the edge of the gate on the drain side.

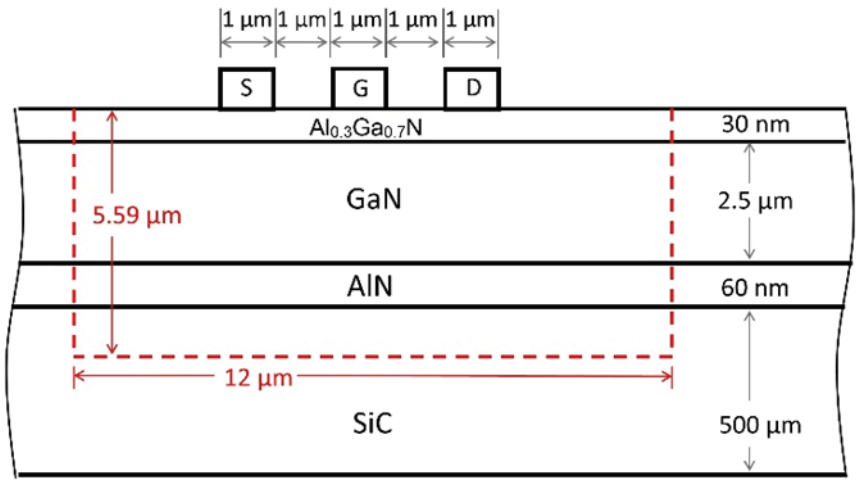

Figure 4: Schematic Diagram of the Cross Section of the Simulated GaN HEMT
Region enclosed by dashed line is the domain for phonon MC simulations.

Figure 5 compares the classic Joule heating with the heat generation rate from electron MC simulations by counting the total energy of emitted phonons per unit time per unit area of 2DEG. The Joule heating is calculated as **J**·**E**, and is the macroscopic version of the energy dissipation of electrons driven by an electric field. Here the current density **J** is obtained at the end of the electron MC simulation. For a small electric field on the left half of Figure 5, Joule heating does not differ largely from the heat generation rate from phonon emission. However, the peak heat-generation rate is overestimated with **J**·**E**. This trend agrees with the early work on Si.[38]

The domain size for phonon MC simulations is chosen as 12 µm long and 5.59 µm deep. Horizontally, the center of the gate aligns with the center of the phonon MC simulation domain. The GaN, AlGaN, and AlN layers, as well as the top 3 µm thickness of the SiC substrate are included in the domain, as shown using dashed line in Figure 4. Compared with majority phonon MFPs of less than 2 µm, the distance between the hot spot and phonon MC domain boundary is sufficiently long so that the Fourier's law becomes valid outside the phonon MC domain. Due to their weak contribution, the thin metal layers of the terminals (i.e., source, drain, and gate) are neglected in the simulation.

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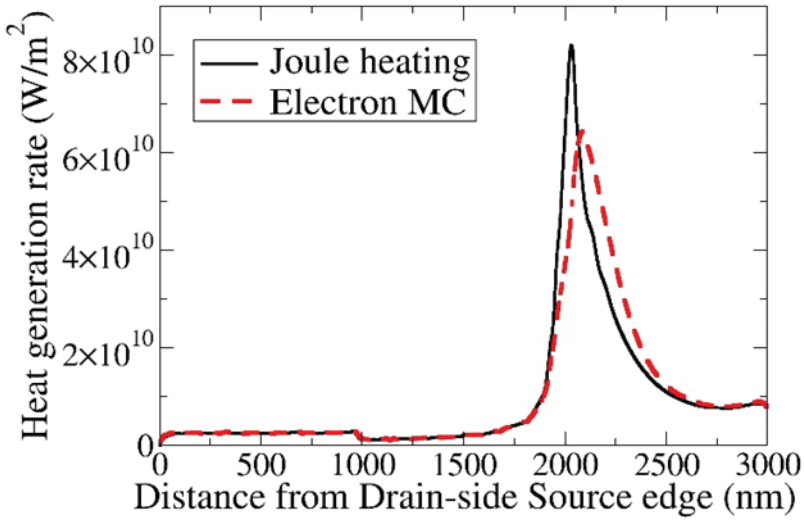

Figure 5: Comparison of the Heat Generation Rate per Unit Area of 2DEG Between Joule Heating (black line) and that due to Phonon Emission Calculated from Electron MC Simulation (red dashed line)

The profile is for the region between gate-side edges of source and drain.

Figure 6(a) shows the acoustic phonon temperature profile in the phonon MC simulation domain after convergence. The hot spot is at the gate edge on the drain side, and the highest temperature is around 490 K. Dotted lines in Figure 6(a) mark the high temperature region of the simulated 2D HEMT, and the time-averaged temperature profile of this region is shown in Figure 6(b).

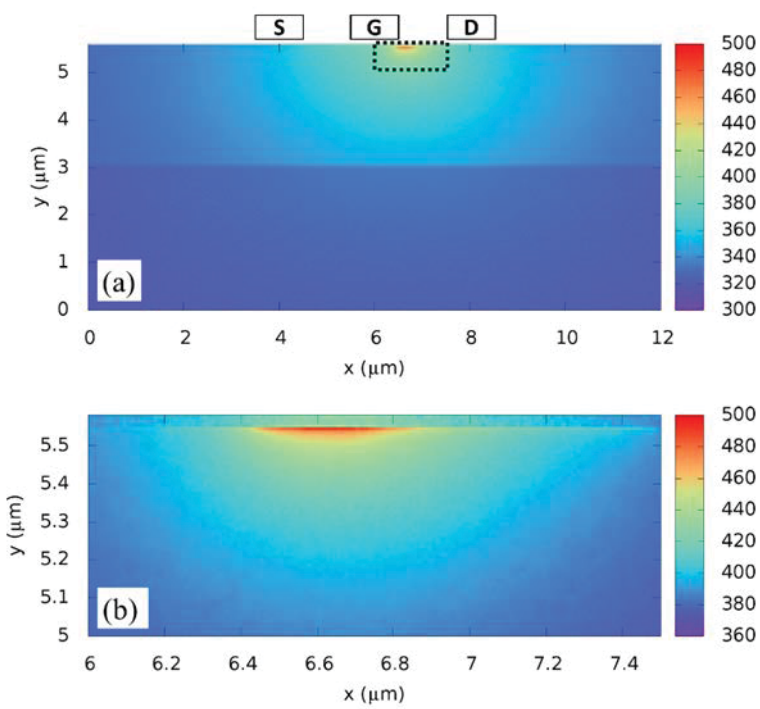

Figure 6: Acoustic Phonon Temperature Profile from Phonon MC Simulation

(a) The whole phonon MC simulation domain and (b) Close-up of hot spot region as enclosed with dotted line in (a).

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Figure 7 compares the acoustic phonon temperature profile along the 2DEG channel, which is evaluated for the GaN subcells on the AlGaN/GaN interface. In the region with heat generation ($4.5 < x < 7.5$ μm), the analysis according to Fourier's law can largely underestimate the hot spot temperatures. This is a general conclusion from all simulations of different GaN transistors.

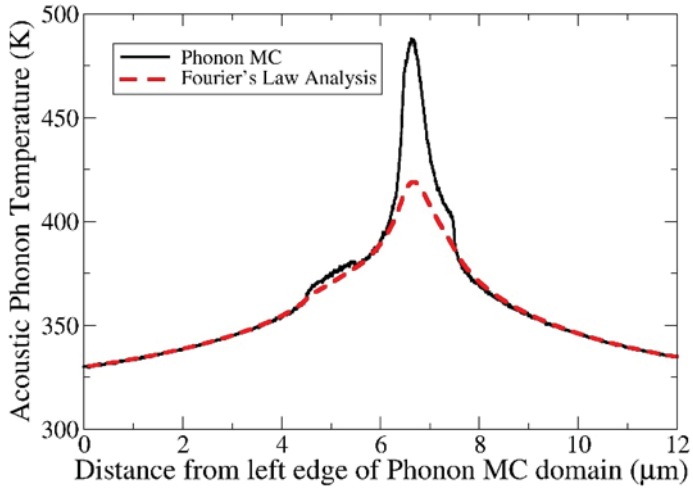

Figure 7: Comparison of the Acoustic Phonon Temperature at the GaN/AlGaN Interface between Phonon MC Simulation (black line) and Fourier's Law Calculation (red dashed line)

4.2 2D GaN HEMT with AlN Heat Spreader

Numerous techniques have been proposed to address the thermal issues of GaN HEMTs. The strategies include microchannel cooling,[8] replacing the SiC substrate with ultra-high-thermal-conductivity diamond, [39,40] adding a heat-spreading layer close to the hot spot,[41-43] etc. In this subsection, the hybrid simulation technique is used to re-evaluate one proposed thermal management strategy, i.e., by coating a heat-spreading layer on top of a GaN HEMT.[41] As a general guidance for the thermal design of a device, the device thermal resistance is also computed as the maximum acoustic-phonon temperature rise within a device divided by the given dissipated power.

The effect of AlN heat spreaders with various thicknesses on top of a HEMT is studied with the hybrid electrothermal simulation technique, and the result is compared with experiments.[41] Figure 8 shows the schematic diagram of the 2D HEMT. The HEMT consists of three layers following the experimental setup.[41] From the top to bottom, they are a 25-nm-thick AlGaN layer, a 2-μm-thick GaN layer, and a 100-μm-thick sapphire substrate. The source, gate, and drain terminals are approximated as thin Au blocks that are 50 nm thick and 1 μm long each. The source-gate separation and the gate-drain separation are both 2 μm. The heat spreader AlN layer has different thicknesses, ranging from 0 to 500 nm. The dashed line in Figure 5 shows the phonon MC domain with its width of 20 μm and its horizontal center aligned with the drain-side gate edge, as the location for the hot spot. In the vertical direction, the phonon MC domain extends from the top of the device to 4 μm depth within the sapphire substrate. The size of the whole chip simulated by ANSYS is about 100 μm×100 μm. With the boundary temperature set to 300 K for the bottom and the two side boundaries, the temperature profile of the whole system

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is simulated using ANSYS, and the computed temperature on the boundary of the phonon MC domain is set accordingly in the phonon MC simulation.

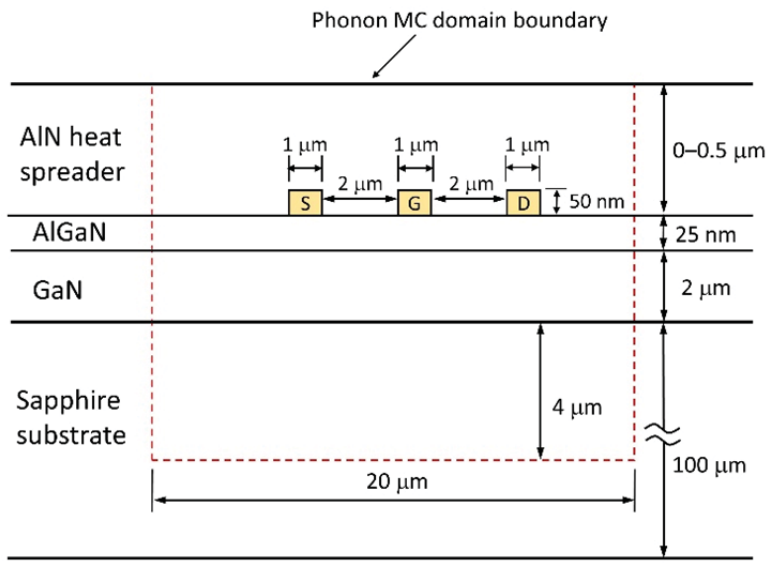

Figure 8: Schematic Diagram of the HEMT being Simulated

The material and size of the HEMT match that of Tsurumi et al., IEEE Trans. Electron Devices 57, 980-985 (2010).[41] The top AlN heat spreader layer has different thicknesses. The red dashed lines are the phonon MC domain boundaries.

Figures 9 (a)-(c) show the temperature profile of the whole chip from the Fourier's law analysis using ANSYS simulations. The applied voltage for the terminals are $V_D = 30$ V for the drain, $V_S = 0$ V for the source, and $V_G = 0$ V for the gate. The k_L of bulk Au is used for the source, gate, and drain terminals. The interfacial thermal resistances are used for the Au/AlGaN and Au/AlN interfaces. For each ANSYS simulation, the overall temperature profile (top) and near-transistor temperature profile (bottom) are shown. The ANSYS calculations show that the hot spot temperature drops about 20 K when the thickness of the AlN heat spreader changes from 100 nm to 500 nm.

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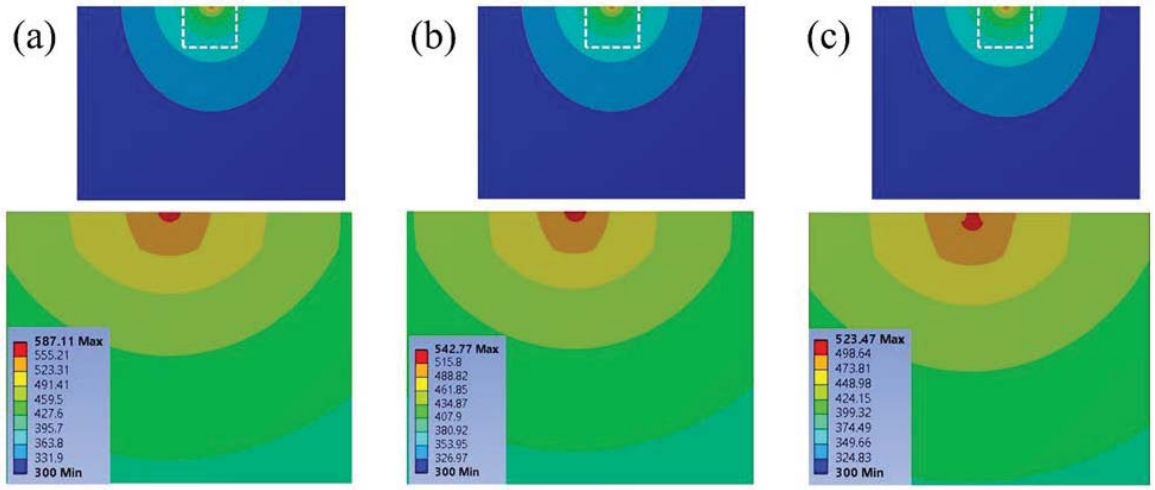

Figure 9: Temperature profiles calculated from ANSYS simulations for AlN thicknesses of (a) 0, (b) 100 nm, and (c) 500 nm

Top profiles are for the whole chip with size of 100 μm×100 μm. The region inside white dashed lines of the top profiles are shown in detail in the bottom profiles.

Figure 10 further shows the temperature profiles from our coupled electron/phonon MC simulations for the three thickness of the heat spreader: 0, 100 nm, and 500 nm. The hot spot temperatures are ~640 K, 590 K, and 570 K, respectively.

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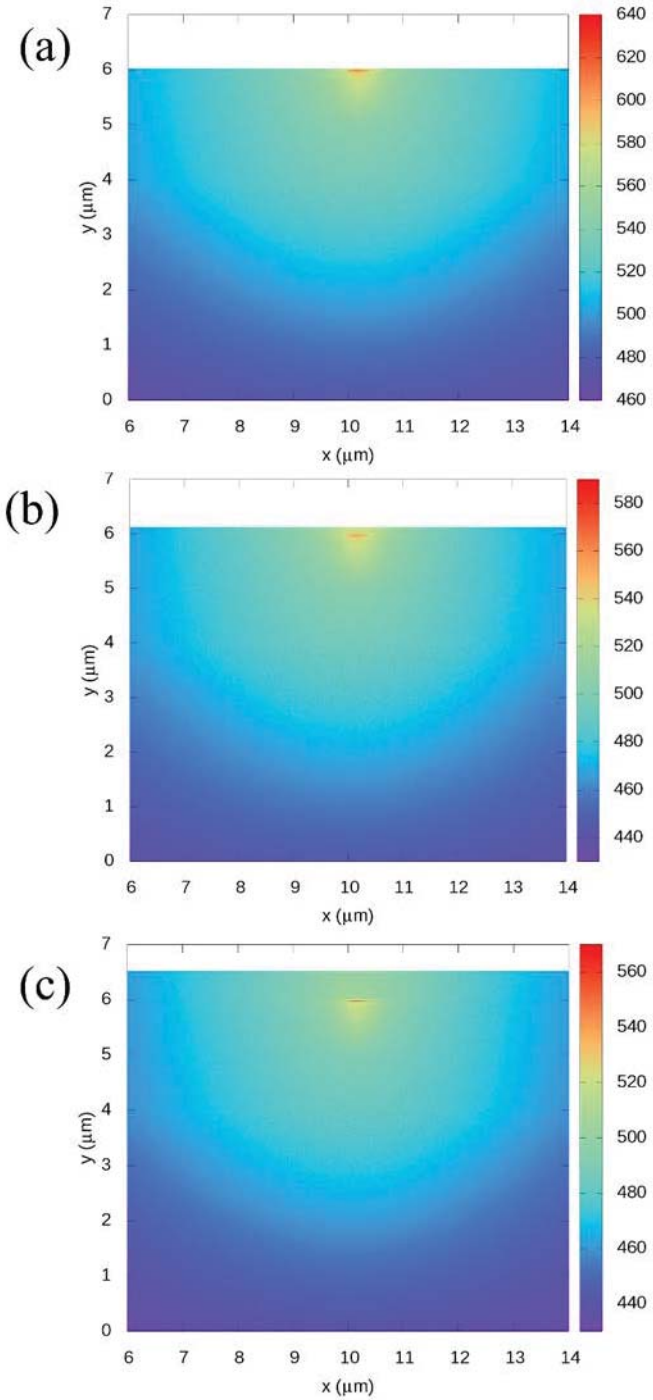

Figure 10: Temperature Profiles given by Coupled Electron and Phonon MC Simulations
The thickness of the AlN coating on top of AlGaN layer is (a) 0, (b) 100 nm, and (c) 500 nm. Only the central part of the phonon MC simulation domain is shown. The origin of the coordinate system is the lower left corner of the phonon MC domain as shown in Figure 8.

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Compared with the result from electron/phonon MC simulations, the hot spot temperature is underestimated by ANSYS simulations. Similar results have been found in early studies on Si transistors using a frequency-independent phonon MFP.[44,45] The divergence is due to the increased importance of ballistic phonon transport at small scales, whereas the Fourier's law assumes completely diffusive phonon transport. Despite the difference, the amount of the hot spot temperature reduction is about the same for ANSYS and electron/phonon MC simulations. For instance, the maximum temperature drops about 50 K after adding a 100-nm-thick layer of AlN in electron/phonon MC simulations, compared with about 45 K in ANSYS. The maximum temperature further drops about 20 K for the AlN thickness increased from 100 nm to 500 nm in electron/phonon MC simulations, similar to the ANSYS result. Experimentally, the rough channel temperature drops about 30 K for thickness changed from 100 nm to 500 nm[41] though large uncertainty is associated with the temperature measurements using the forward voltage of the source-drain diode. Nevertheless, the hybrid electrothermal MC simulation confirms that adding heat spreader can significantly reduce the hot spot temperature.

One of the important thermal characteristics of a device is the "device thermal resistance," defined as the maximum temperature rise in a device divided by the power dissipation in the device. For GaN HEMTs, the device thermal resistance has been studied using a simplified model, where a GaN/substrate combination was used as a HEMT.[46] In this study, the Fourier's law was used for heat transfer. The thermal boundary resistance at the GaN/substrate interface was determined to be the main contributor to the device thermal resistance, which has been proposed by other studies.[47,48] However, Fourier's law analysis for heat conduction does not consider optical phonons in the calculation of device thermal resistances. When the thermal nonequilibrium between three thermodynamic systems (electrons, optical phonons, and acoustic phonons) are considered, the device thermal resistance is re-defined as the maximum acoustic-phonon temperature rise divided by the total power dissipation. With the applied voltage $V_D = 30$ V, $V_S = 0$ V and $V_G = 0$ V, Figure 11 shows the temperature profiles of above thermodynamic systems along the channel, where the hot electron temperature can be up to 10000 K and is orders of magnitudes higher than the acoustic phonon temperature. Using the hybrid electrothermal simulation, acoustic phonon temperatures can be accurately determined for the computation of the device thermal resistance.

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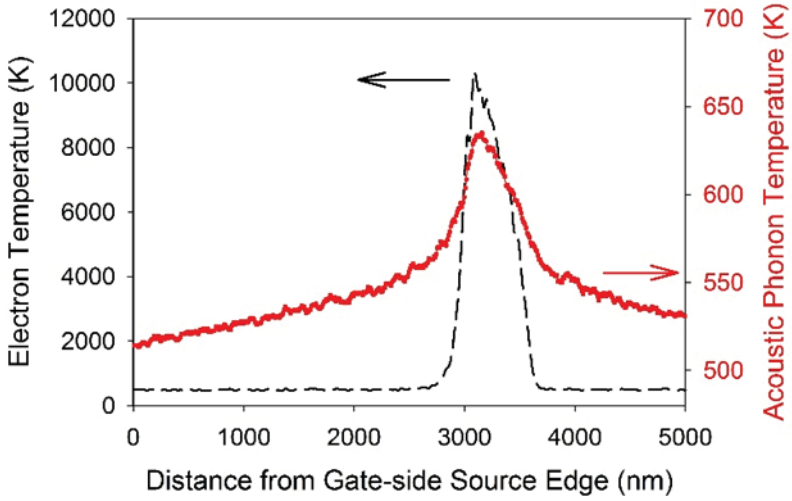

Figure 11: Electron and Phonon Temperature Profiles along the 2DEG Channel between the Source and Drain

The dashed black line using the left y-axis is the electron temperature from the electron MC simulation. The red solid line using the right y-axis is the acoustic-phonon temperature from the phonon MC simulation. The applied voltages are $V_S = V_G = 0$ V and $V_D = 30$ V.

For the simulated HEMT device with varied drain voltage V_D and fixed $V_G = V_S = 0$ V, the relation between the maximum temperature rise in device and the input power density is shown in Figure 12(a). The slope of the curve in Figure 12(a) is the device thermal resistance that is shown in Figure 12(b) as a function of the drain voltage V_D. In both figures, the solid black line is the result calculated with the maximum acoustic-phonon temperature rise from coupled electron/phonon MC simulations, and the dashed red line is calculated from ANSYS simulations. Device thermal resistances calculated by both methods do not show linear behavior with the drain voltage. The increased device thermal resistance at high drain voltages results from the reduced thermal conductivities of involved material layers above 300 K.

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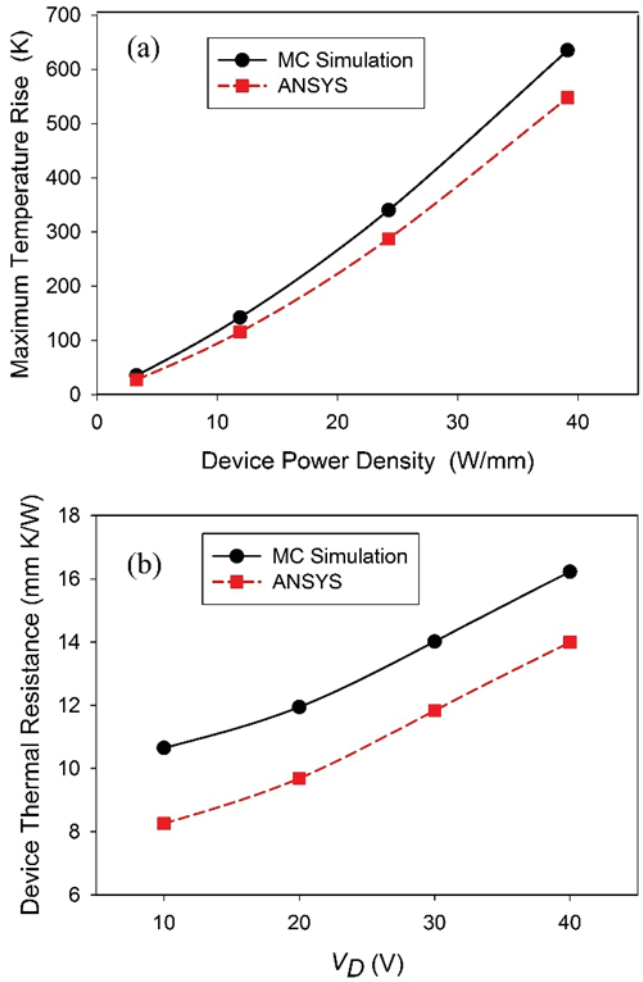

Figure 12: (a) Maximum Temperature Rise of the Modeled HEMT for Different Input Power Density and (b) Calculated Device Thermal Resistance per Unit Channel Width of the Modeled HEMT at Different Drain Voltage V_D while Keeping $V_S = V_G = 0$ V

The solid black lines are calculated using the maximum acoustic-phonon temperature rise from MC simulations, and the dashed red lines are calculated with the maximum temperature rise from ANSYS simulations.

4.3 3D GaN FinFET Array on SiC Substrate

Coupled electrothermal simulation is performed on a 3D GaN-on-SiC FinFET array. Following the experimental setup,[2] Figure 13 presents the simulated FinFETs using 31 parallel Si-doped GaN nanowires. To reduce the computational load, one nanowire in the middle is chosen for the study and the phonon MC domain is indicated by dot-dashed lines A and B in Figure 13(b). The distance from the hot spot to the boundary of this domain is 6–10 µm, which is longer than majority phonon MFPs in GaN and SiC[13] to validate the Fourier's law analysis outside the phonon MC domain. On both sides (at dot-dashed lines A and B in Figure 13(b)) of the phonon MC domain, specular phonon reflection is enforced due to structure symmetry.[49] Although this boundary condition is inaccurate for the two nanowires on the edge of the nanowire array, limited influence is anticipated for a nanowire in the middle of the array and the computational load can be largely minimized with the proposed computational domain.

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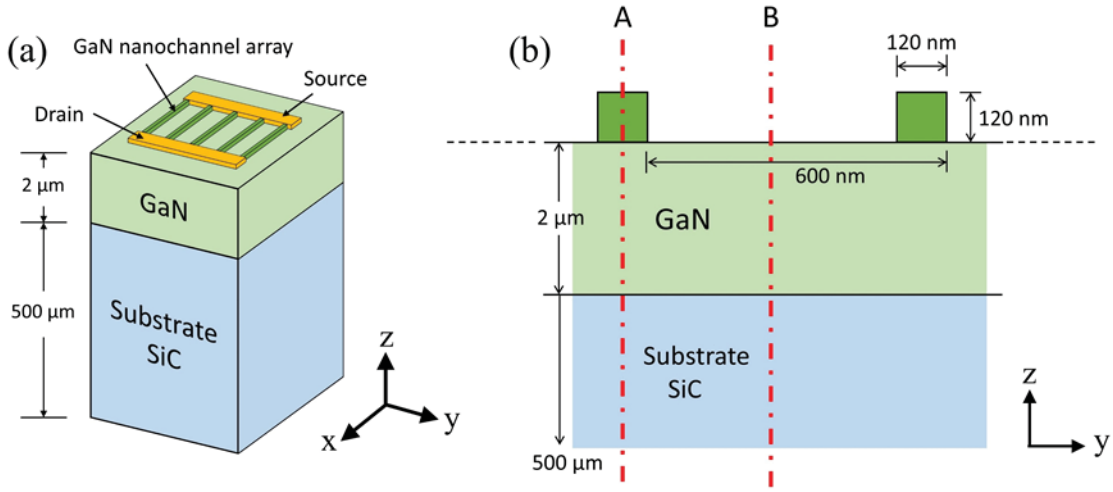

Figure 13: Schematics of the Simulated 3D GaN-on-SiC Device
(a) 3D structure and (b) cross-sectional view perpendicular to the GaN FinFETs.

Since electron current happen in the nanochannel/fin region, which is also where electron-phonon scattering occurs and heat was generated, the electron MC domain only includes the (half) nanochannel. The dimension of the electron MC domain is 3 µm × 60 nm × 120 nm, and the size of the cell for electron MC is set to be 20×20×20 nm^3. The size of the phonon MC simulation domain is 15 µm × 300 nm × 6.12 µm, as shown in Figure 14.

Figure 15 shows the simulated acoustic phonon temperature distribution of the FinFET device, both in a side view and a top view. The temperature distribution on the top side of the GaN nanowire is plotted in Figure 16, where the results of Fourier's law analysis and coupled MC simulation are compared. The temperature difference is shown in Figure 16(a). Here again, in the hot spot region, Fourier's law fails to predict the correct temperature. The difference can be as large as 35 K.

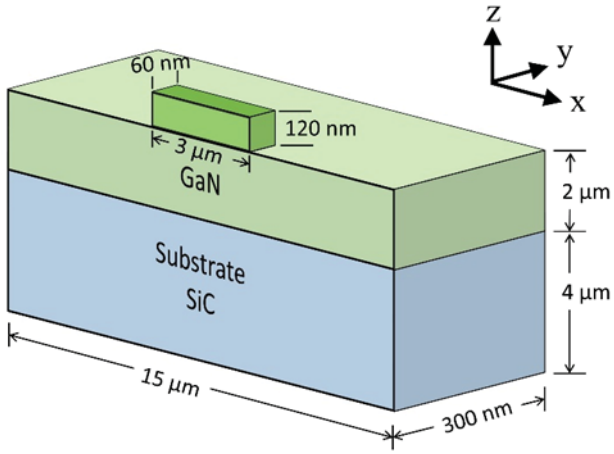

Figure 14: Phonon MC Simulation Domain for the 3D GaN-on-SiC FinFET Array

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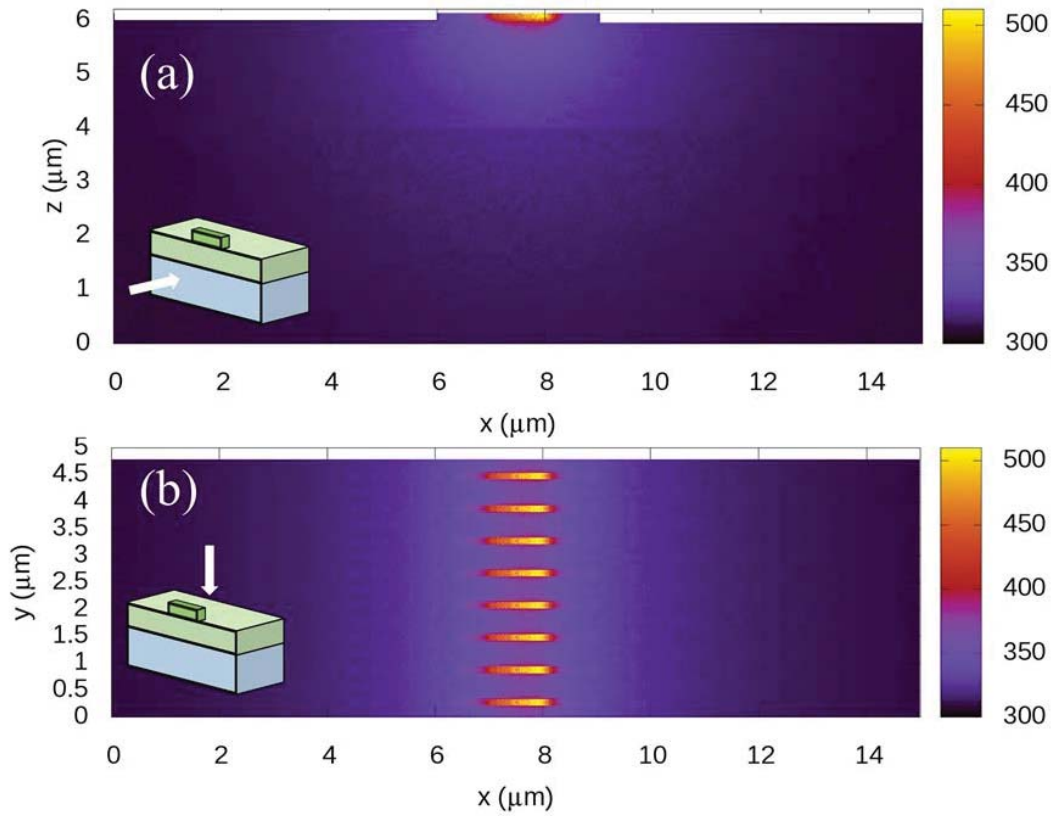

Figure 15: (a) Side View (at mirror symmetry plan A) and (b) Top View of Temperature Profile (in K) from Coupled Electrothermal Simulation of the GaN-on-SiC FinFET Array

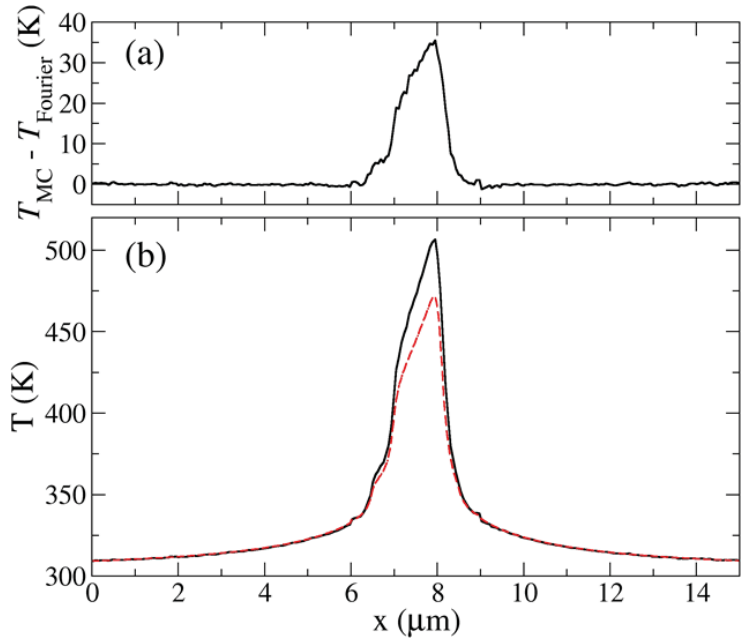

Figure 16: Temperature Profile on the Top Side of GaN Nanowire of GaN-on-SiC FinFET
(a) temperature difference between phonon MC simulation and Fourier's law analysis and (b) temperature from MC simulation (solid line) and Fourier's law analysis (dashed line).

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4.4 Thermal Studies of Nanoporous $In_{0.1}Ga_{0.9}N$ Films

In addition to existing efforts on thermal management, on-chip thermoelectric (TE) cooling can be more effective because heat can be directly and effectively removed from the hot spot. To integrate such TE coolers with a GaN HEMT, the selected TE materials should have a thermal expansion coefficient similar to that for GaN for better compatibility. Correspondingly, GaN-based alloys are recommended for such TE devices.[50] In physics, the effectiveness of a TE material is evaluated by its dimensionless TE figure of merit (ZT), defined as $ZT = S^2\sigma T/k$, where S, σ, k, and T represent the Seebeck coefficient, electrical conductivity, thermal conductivity, and absolute temperature, respectively. For GaN alloys, the power factor $S^2\sigma$ can be better than those for the state-of-the-art high-temperature TE materials such as Si_xGe_{1-x} alloys.[51] The major challenge lies in how to reduce the intrinsically high k but still maintain the high power factor.

As one potential direction proposed in our proposal, some efforts have been dedicated to TE studies of GaN alloys, with a focus on k reduction by nanoporosity introduced to the corresponding thin films. In these nanoporous thin films, phonons with long wavelengths and MFPs can be further scattered by the nanopore edges, as the classical phonon size effect. On the other hand, electrons typically have a much shorter MFP in GaN alloys (~10 nm or less) and are less affected by the same nanoporous structure. This allows decoupling of electron and phonon transport for ZT enhancement. Figures 17a and 17b show the scanning electron microscopy (SEM) images of representative nanoporous films.

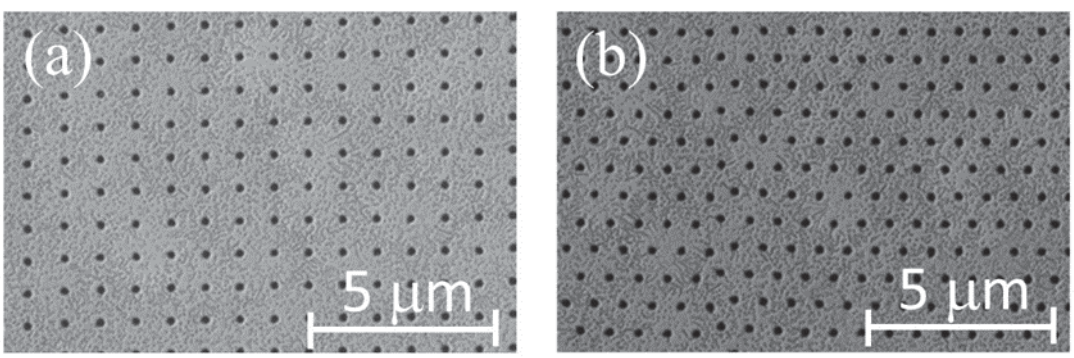

Figure 17: SEM Images of the as Prepared Nanoporous $In_{0.1}Ga_{0.9}N$ Films with (a) Aligned Pores or (b) Hexagonally Aligned Pores

Different from reported nanoporous Si films with pores fabricated by reactive ion etching,[52-57] our $In_{0.1}Ga_{0.9}N$ films were directly grown on the substrate, with the nanopores defined by SiO_2 pillars as masks. For all patterns, the pore diameters were fixed at 300 nm and the pores were located on either a square lattice or hexagonal lattice. All layers were grown with unintentional doping. Prior to growth, the sapphire substrate was heated in H_2 ambient at 1000℃ for 3 min to remove surface contaminations. The growth of the structure began with a 50-nm-thick low temperature GaN nucleation layer grown at about 500ºC for 3.5 min. Following this, a 50 nm GaN buffer layer was grown at 1060℃ for 1 min. Afterwards, the growth was completed by deposition of 150 nm $In_{0.1}Ga_{0.9}N$ layer at 805℃ for 60 min. After the high-temperature growth, SiO_2 nanopillars were removed with hydrogen fluoride to obtain the nanoporous pattern. In

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contrast with nanofabricated pores, directly grown nanopores have minimized pore-edge defects to eliminate the influence of amorphous pore edges on *k*, as proposed for nanoporous Si films.[58]

Cross-plane *k* has been measured for fabricated $In_{0.1}Ga_{0.9}N$ thin films via the time-domain thermoreflectance (TDTR) method. TDTR is an optical-based, accurate, and robust technique applicable of probing various thermal properties, including thermal conductivity, interfacial thermal conductance, and heat capacity of sample systems ranging from thin films, bulk substrates, to nanoparticles. Prior to thermal measurements, a 55-nm-thick layer of aluminum was coated onto the whole wafer by electron beam deposition to serve as the optical transducer.

Figure 18 shows the measured cross-plane *k* (symbols) compared to phonon transport modeling (line) assuming bulk phonon MFPs and diffusive pore-edge phonon scattering. The uncertainty due to thermal penetration into the substrate is indicated with error bars. In general, the experimental data agree well with the modeling.

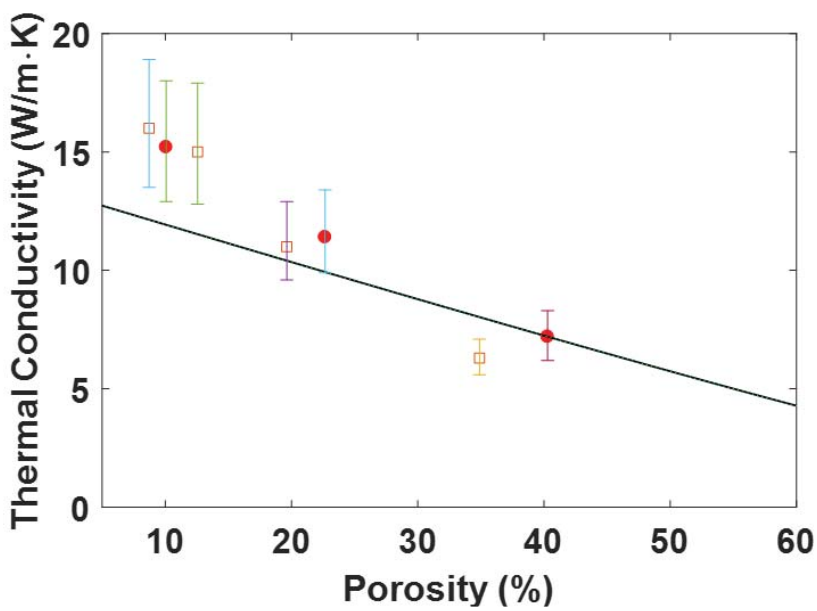

Figure 18: Comparison between the Measured and Predicted *k* Values for Tri-layered Nanoporous GaN-based Films

Here filled circles are for hexagonal patterns, whereas empty squares are for patterns on a square lattice.

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5. CONCLUSIONS

An efficient and accurate multi-length scale hybrid simulation technique has been developed to assess the over-heating problem of high-power GaN devices. The electron MC simulation is used to characterize the energy transfer from electrons to phonons. Within the transistor region, the deviational phonon MC simulation is used to get the lattice temperature, where the Fourier's law is known to fail at such small scales. Away from the hot spot, the Fourier's law can be employed to characterize the heat spreading across a macroscale device.

In demonstration, 2D GaN HEMTs are simulated. The electric field is found to peak at the drain-side gate edge, where the hot spot coincides. The Fourier's law analysis significantly underestimates the hot spot temperature. As one thermal management strategy for GaN devices, the use of AlN heat spreader on top of the AlGaN layer in a GaN HEMT is studied. The use of AlN heat spreader can decrease the HEMT surface temperature by tens of Kelvins. In addition, the device thermal resistance is computed as the maximum acoustic-phonon temperature rise divided by the total energy transfer rate from hot electrons to phonons. Again the estimation using the Fourier's law is found to be less accurate. For an array of 3D GaN FinFETs, coupled electron and phonon MC simulation in 3D structures is performed. The 3D electric field is found to peak at the drain-side gate edge, similar to that for a 2D HEMT. The Fourier's law is again found to underestimate the temperature rise at the hot spot. In general, the hybrid electrothermal simulation is accurate and versatile, and can provide important guidance for the improved thermal designs of GaN devices.

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6. GOALS AND ACCOMPLISHMENTS

Goal	Status
• (Task 1) Develop MC simulation that can predict phonon generation along 1D nano-channel	done in Report 1
• (Task 1) Reproduce electron drift velocity vs. electric field and temperature, compare with literature	done in Report 1
• (Task 2) Incorporate phonon frequency dependency into phonon MC for 3D transistor	done in Report 4
• (Task 2) Couple MC with conventional Fourier analysis	done in Report 3
• (Task 2) Show temperature distribution across device	done in Report 3
• (Task 3) Parallel electron MC computations	done in Report 3
• (Task 3) Deviational phonon MC technique	done in Report 2
• (Task 4) Electromagnetic thermal simulation	done in Report 8
• (Task 5) Simulation Confirmation	done in Report 6

For publications, one book chapter is published. One article on general electrothermal simulations of 2D HEMTs is published in *J. Appl. Phys*. One manuscript on the simulation of thermal management strategies of HEMTs with AlN coating is under review. One manuscript on 3D GaN FinFETs is being submitted. One more manuscript on vertically aligned gate-all-around FinFETs is under preparation. As an extension of this project, one paper on the thermal studies of nanoporous $In_{0.1}Ga_{0.9}N$ films is accepted, which provides important guidance for TE cooling of GaN devices.

The updated research progress was presented in May 2016 (invited talk at the 3rd International Conference on Photonics and Thermal Energy Science, Xi'an, China), July 2016 (the 4th International Conference on Computational Methods for Thermal Problems, Georgia Institute of Technology), November 2016 (IMECE 2016 conference, Phoenix, AZ), and March 2017 (MRS 2017 Spring Meeting, Phoenix, AZ).

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LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
BTE	Boltzmann transport equation
FET	field effect transistor
HEMT	high electron mobility transistor
LO	longitudinal optical
MC	Monte Carlo
MFP	mean free path
SEM	scanning electron microscopy
TDTR	time-domain thermoreflectance
TE	thermoelectric

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